UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/624,509	07/23/2003	Isao Takayanagi	M4065.0905/P905	7407

24998 7590 11/12/2008

DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC 20006-5403

EXAMINER	
TRAN, NHAN T	
ART UNIT	PAPER NUMBER
2622	

MAIL DATE	DELIVERY MODE
11/12/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/624,509	TAKAYANAGI, ISAO	
	Examiner	Art Unit	
	NHAN T. TRAN	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 August 2008 and 17 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-11,51-55,57-59 and 62-66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *51* is/are allowed.

6)☒ Claim(s) *1-4, 6-11, 52-55, 57-59 and 62-66* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/13/2008 and 7/17/2008 has been entered.

Response to Arguments

2. Applicant's arguments filed 7/17/2008 have been fully considered but they are not persuasive.

The Applicant argues that:

(1) In the invention of Iwai, black reference noise is removed from the video stream. The black reference noise data is collected from a portion of the CCD imager that collects data when "no light is incident on the CCD." (Iwai col. 6, In. 26-44). The section of the CCD imager which generates the noise signals is blocked from receiving light (Fig. 7). Accordingly, the dark shading signal of Iwai does not relate to noise caused by the non-uniformity of illumination or optical shading. Thereby, Iwai fails to teach *"a pixel array circuit that outputs an image signal including a background signal caused by at least one of non-uniformity of illumination and optical shading,"* as recited

in independent claim 1 and *"a pixel array circuit for outputting an image signal including a background only signal caused by at least one of non-uniformity of illumination and optical shading,"* as recited in independent claim 52.

(2) Dai discloses the reference image is processed using Fast Fourier Transforms (FFT) to determine what filter to apply to the reference image. After the filter is applied to the reference image, the resulting signal is subtracted from the target image. Accordingly, the signal which is output from the CCD imager is not subtracted from the image signal (i.e., target signal) but is processed (FFT and filtered) and the filtered image is subtracted from the image signal. Accordingly, Dai fails to teach "a pixel array circuit that outputs an image signal including a background signal...a data subtraction circuit, coupled to said memory array circuit and said pixel array circuit, said data subtraction circuit performing a data subtraction operation on the pixel array output to remove said background signal from said image signal," as recited in independent claim 1 and "a pixel array circuit for outputting an image signal including a background only signal...a data subtraction circuit, coupled to said memory array circuit and said pixel array circuit for performing a data subtraction to remove said background only signal from said image signal using said stored background signal," as recited in independent claim 52.

(3) Goren fails to discuss a pixel signal having a background signal, and thus fails to make up the deficiencies of Iwai.

In response, the Examiner understands the Applicant's arguments but respectfully disagrees with the Applicant's assessment of the claims for the following reasons:

(1) It is clearly seen in the claim that the background is caused by optical shading. In Iwai, the optical black pixels (OB pixels) are representing "optical shading" since there is no incident light passing through the shielding layer of the pixels (col. 6, lines 1-4, 25-44). In a broad sense, the optical black pixels cause to generate the background noise signal that is used as a reference noise signal to subtract from image signal to remove noise at a subsequent step. Thus, the background signal is caused to be generated by the optical black pixels corresponding to "optical shading" in a broad interpretation. The Examiner notes that the claims are written broad enough to read on the disclosure of Iwai since the "optical shading" is recited too broad.

(2) As disclosed in Dai, the fixed pattern noise (background signal) is caused by one of **optically created noise, optical aberration noise in col. 1, lines 32-42**. As addressed in the previous Office Action, **the background signal is the fixed pattern noise signal** that is inherently included in the target image signal due to the optically created noise or optical aberration noise as mentioned above. Dai teaches that the fixed pattern noise is extracted in step 72 of Fig. 2, and then the noise is removed by subtraction with the target image (see col. 4, lines 11-21). Furthermore, the claimed "background signal" can be interpreted in two different ways. In Dai, the background signal is considered as either the fixed pattern noise or the reference image of a flat, smooth surface. Although the reference image and target image are processed under

Fast Fourier Transform (FFT), they are still considered as the background signal and target image signal since the claims do not require that the background signal is not filtered or processed under FFT. Therefore, the claimed limitations are met by Dai in two different interpretations. For all other limitations of the claims such as data subtraction and memory array, please refer to the previous Office Action mailed 4/17/2008 or the rejection section below.

(3) Since Iwai has met the claimed limitations as discussed above, the combined teaching of Iwai and Goren also stands.

In view of the above, the rejection is maintained.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 4, 52, 55, 62 & 65 are rejected under 35 U.S.C. 102(b) as being anticipated by Iwai (US 6,072,527).

Regarding claim 1, Iwai discloses an imaging device (Fig. 1 & 2), comprising:

a pixel array circuit (CCD 6 shown in Fig. 1 and details in Fig. 6) that outputs an image signal including and a background signal (OB signal) caused by at least one of non-uniformity of illumination and optical shading (Figs. 6 & 7; see col. 5, line 63 – col.

6, line 44, wherein optical shading is represented by the shading of the optical black pixels);

a memory array circuit (sample and hold array circuit 7a and 7b in Fig. 1 inherently contains memory/buffer array in order to sample and hold the signal), coupled to said pixel array circuit, to store the background signal (col. 8, lines 6-20);

a data subtraction circuit (subtracter 8 in Fig. 1), coupled to said memory array circuit and said pixel array circuit, said data subtraction circuit performing a data subtraction operation on the pixel array output to remove said background signal from said image signal (see col. 8, lines 6-47).

Regarding claim 4, it is also seen from Fig. 1 of Iwai that each memory element in said memory array (7a & 7b) corresponds to a pixel circuit in said pixel array circuit (it should be noted that each pixel circuit of CCD 6 is connected to the sample and hold array 7a & 7b, thus each pixel array circuit corresponds to the memory array element in a broad sense).

Regarding claims 52 & 55, these claims are also met by the analysis of claims 1 & 4, respectively.

Regarding claims 62 & 65, as disclosed by Iwai in col. 7, lines 9-15, the background signal also includes a dark signal which imposes a fixed pattern noise by inherency.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 52, 62-65 are rejected under 35 U.S.C. 102(e) as being anticipated by Dai et al. (US 6,763,142).

Regarding claim 1, Dai discloses an imaging device (Fig. 1), comprising:

a pixel array circuit (CCD array 20) that outputs an image signal including and a background signal caused by at least one of non-uniformity of illumination and optical shading (the target image inherently contains optical aberration noise known as non-uniformity of illumination or optical shading; see col. 1, lines 35-37 and col. 5, lines 14-31);

a memory array circuit (24 in Fig. 1), coupled to said pixel array circuit, to store the background signal;

a data subtraction circuit (27 in Fig. 1), coupled to said memory array circuit and said pixel array circuit, said data subtraction circuit performing a data subtraction

operation on the pixel array output to remove said background signal from said image signal (see col. 1, lines 6-10; col. 4, lines 11-17 and col. 5, lines 45-56).

Regarding claim 52, this claim is also met by the analysis of claim 1.

Regarding claims 62 & 65, Dai clearly discloses that the background signal further comprises a fixed pattern noise signal (col. 4, lines 11-17).

Regarding claims 63 & 64, Dai also discloses that the background signal, collected from the pixel array circuit, is captured from a no-data of a memory disk (col. 4, lines 32-40, wherein the short term memory 24 shown in Fig. 1 represents the memory disk, and the fixed pattern noise is stored in a no-data of the memory by inherency because signal can only be stored in a no-data area (empty area) of the memory).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2, 3, 6-11, 53, 54, 57-59 & 66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwai (US 6,072,527) in view of Goren et al. (US 5,734,152).

Regarding claim 2, Iwai does not teach an image enhancement circuit that performs an edge enhancement operation on the image signal received from the data subtraction circuit.

However, as taught by Goren, an edge enhancement filter (30 in Fig. 2a) is provided in an analog domain after a differentiator circuit (4) but before a digital circuit (20 in Fig. 1a) so that the edges of captured image signal are much more pronounced and it is much easier to digitize and decode such an enhanced signal (see col. 6, lines 54-57 and col. 8, lines 15-18).

Therefore, it would have been obvious to one of ordinary skill in the art to implement an analog edge enhancement circuit after the subtraction circuit and prior to ADC circuit in Iwai so that the edges of captured image signal are much more pronounced and it is much easier to digitize and decode such an enhanced signal as taught by Goren.

Regarding claim 3, Iwai in view of Goren also discloses that the imaging device comprises an analog-to-digital converter (20 in Fig. 1a of Goren) which converts the signal received from the image enhancement circuit to a digital signal.

Regarding claim 6, the combined teaching of Iwai and Goren as discussed in claim 1 also meets the method claim 6 except for "an imager chip" that is understood as an integrated imaging circuit for implementing the method. However, an Official Notice

is taken that it is notoriously well known in the art to integrate an image sensor with image processing modules into a single chip for reducing size of circuitry for a compact apparatus. Therefore, it would have been obvious to one of ordinary skill in the art to construct an imager chip that would implement the method for processing the image data as claimed to reduce circuit size, thereby providing a compact apparatus.

Regarding claim 7, Iwai and Goren as discussed in claim 6 further discloses that the analog image data is received from a pixel array (CCD 6 in Iwai) in said imager chip.

Regarding claim 8, Iwai and Goren as discussed in claim 6 also discloses that the analog image data is received from a memory array (sample and hold circuit 7a & 7b in Iwai) in said imager chip.

Regarding claim 9, it is seen from Iwai that the optical black signal in Iwai is considered as an offset variation signal since it is used as an offset to remove the dark shading (col. 7, lines 9-15).

Regarding claim 10, as disclosed by Iwai, the background signal also includes a dark current which imposes a fixed pattern noise by inherency (see Iwai, col. 7, lines 9-15).

Regarding claim 11, this claim is also met by the analysis of claim 3.

Regarding claims 53 & 54, these claims are also met by the analyses of claims 2 & 3, respectively.

Regarding claim 57, this claim is also met by the analyses of claims 1 & 6 above, wherein "an integrated circuit" is the imager chip and "a substrate" is inherent (i.e. silicon substrate) in the imager chip.

Regarding claims 58, 59 & 66, these claims are also met by the analyses of claims 2, 3 & 10, respectively.

Allowable Subject Matter

7. Claim 51 is allowed.

The reason for allowance can be found in the Applicant's remarks filed 1/4/2008.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to NHAN T. TRAN whose telephone number is (571) 272-7371. The examiner can normally be reached on Monday - Friday, 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lin Ye can be reached on (571)272-7372. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/NHAN T TRAN/
Primary Examiner, Art Unit 2622